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CS 6960.001

Assignment 3 Analysis

Analysis:

1.

- L1 hit + hit under miss rate := (hit under miss + L1 hits)/L1 accesses. Value for chip found in previous assignment: (379+8272480)/8322060 ≈ 0.9941

- Energy consumption when L1 disabled: 0.059429J
  Energy consumption when L1 enabled: 0.039675J
  When the L1 is enabled, LOADs can often be serviced by the L1 instead of DRAM. DRAM accesses are more expensive, so L1 saves energy.

- Adding the L1 allowed some functional unit bottlenecks. I doubled BLT 2 to 4, FPMIN 4 to 8, and FPCMP 2 to 4. The L1 configuration "L1 1 16384 8 4" worked pretty well. FPS/area: 229.8741/2.492 ≈ 92.2461

2. The L2 didn't have a great hit rate, since the L1 is so good. Still, it gave a noticeable performance boost and energy usage reduction. Perf/area went from 1182.7223/39.8714 ≈ 29.6634 to 1232.6428/45.8317 ≈ 26.8950 while power/area went from ~50.6790W to ~41.3316W while performance climbed from ~1183 FPS to 1233 FPS. So, it makes sense to use this L2 if we're concerned about power or performance, and not if we're concerned with fab costs.

3. Unfortunately, due to a problem with the simulator, I could not run my code. However, the access patterns in the programs written should be near-optimal for goodness/badness.